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PTO/SB/08A (08-00)

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

### Complete If Known

Application Number	
Filing Date	12/17/2003
First Named Inventor	Madurawe, Raminda U.
Group Art Unit	
Examiner Name	
Attorney Docket Number	

### U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
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### FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
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Application Number				Filing Date	
First Named Inventor				Group Art Unit	
Examiner Name				Attorney Docket Number	
Sheet	2	of	2		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA.	<input type="checkbox"/>
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